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A Soft-Switched Modulation for a Single-Phase Quasi-Z-Source Integrated Charger in Electric Vehicle Application

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ABSTRACT

A new triple voltage boosting switched-capacitor multilevel inverter (SCMLI) is presented in this paper. It can produce 13-level output voltage waveform by utilizing 12 switches, three diodes, three capacitors, and one DC source. The capacitor voltages are self-balanced as all the three capacitors present in the circuit are connected across the DC source to charge it to the desired voltage level for several instants in one fundamental cycle. A detailed comparative analysis is carried to show the advantages of the proposed topology in terms of the number of switches, number of capacitors, number of sources, total standing voltage (TSV), and boosting of the converter with the recently published 13-level topologies. The nearest level control (NLC)-based algorithm is used for generating switching signals for the IGBTs present in the circuit. The TSV of the proposed converter is 22. Experimental results are obtained for different loading conditions by using a laboratory hardware prototype to validate the simulation results. The efficiency of the proposed inverter is 97.2% for a 200 watt load**.**

Keywords: switched-capacitor; voltage boosting; multilevel inverter; nearest level control; modulation index

INTRODUCTION

In recent times, multilevel inverters (MLIs) have been used as a potential solution for DC to AC conversion for various applications such as renewable energy conversion systems, high power drives, a high-voltage direct current (HVDC) transmission system, a distributed power generation system, etc. The main advantages of MLIs are lower dv/dt stress, higher operating voltage with lower rating devices, and near to sinusoidal output voltage, which in turn reduces total harmonic distortion (THD) and fault-tolerant capability [1–3]. Conventional MLIs such as the neutral point clamped (NPC) inverter, flying capacitor (FC) inverter, cascaded H-bridge (CHB) inverter, and modular multilevel converter (MMC) have replaced the conventional two-level inverter for medium and high voltage applications [4,5]. However, these conventional MLIs require more components and more complex control circuitry due to voltage balancing issues with an increased number of levels at the

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output voltage. To overcome these issues, researchers have proposed a self-balanced switched-capacitor multilevel inverter (SCMLI), which can synthesize the desired voltage levels at the output using fewer components and reduced control complexity [6–12]. Several SCMLIs has been presented by researchers utilizing fewer components to realize the desired multilevel output voltage. A seven-level inverter is proposed in [13], which utilizes 10 switches and one capacitor to produce 1.5 times voltage gain. Authors in [14] have used 12 switches and two capacitors to generate seven-level output voltage with increased voltage gain. Recently, several high gain SCMLIs were proposed which are capable of producing 13-level output voltage [15–21]. Four DC sources and 10 switches are used to produce 13-level output voltage in [18] with unity voltage gain. To improve the voltage gain and to reduce the number of sources, [22] uses only one DC source for producing 1.5 times voltage boosting, while [16] uses two sources to achieve dual voltage boosting with an increased number of switches. In [23] a high-voltage boosting of six is achieved, but the number of switches used in the circuit is twenty-nine with a total standing voltage (TSV) of 34. To reduce the number of switches, the authors in [19] used 19 switches for generating voltage boosting of six, but the TSV of the inverter circuit increased to 39. A detailed review on the recently published multilevel inverter topologies to find the most suitable applications with reduced device count is published in [7–12]. In the case of lower solar PV voltages, a high gain DC–DC converter along with multilevel inverter can be used to boost the PV voltage for obtaining desired output voltage for grid integration [24–26]. In this paper a triple voltage gain SCMLI topology is proposed with reduced component count and reduced TSV. The number of switches used in the proposed circuit is 12, with reduced TSV to 22. A simpler NLC based algorithm is used to generate switching pulses for IGBTs employed in the proposed circuit. The main objectives of the proposed topology are as follows; (a) A 13-level output voltage is synthesized with 11 switches and one DC source. (b) The proposed topology provides triple voltage boosting at the output. (c) Total standing voltage (TSV) of the proposed topology has significantly reduced. (d) Negative voltage levels are generated without using an H-bridge. (e) All three capacitor voltages are

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self-balanced, hence control circuitry is simpleWith the use of switched capacitors, a switched-capacitor (SC) inverter may produce voltages at varying levels [9], [10]. In terms of topology, a SC inverter is analogous to a charge pump. This inverter is a kind of SC inverter.

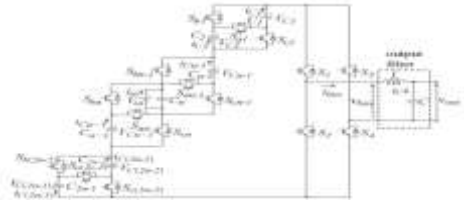

Fig. 1. Circuit topology of the switched-capacitor inverter using series/ parallel conversion.

like the charge pump, it produces an output voltage that is higher than the input voltage. However, the SC inverter's complexity stems from the presence of several switching components. However, an alternative to the SC inverter was offered in the form of a Marx inverter [11], which uses fewer switching elements. The operating concept of the Marx inverter makes it comparable to that of the SC inverters.

In this work, we suggest a SC inverter with a more straightforward design than the standard SC inverter. It is made up of an H-bridge and a Marx inverter construction. By rapidly switching the capacitors between series and parallel, the suggested inverter may provide an output voltage higher than the input voltage. There are no inductors in the suggested inverter, which reduces the size of the system. The suggested inverter's multilayer output helps to mitigate the harmonics at the device's output.

The circuit architecture and driving mechanism are presented in Section II. Capacitance measurement techniques are discussed in further detail in Section III. The predicted and computed losses of the proposed inverter are shown in Section IV.

Results from MATLAB/ SIMULINK simulations and the circuit tests are shown in Sections V and VI, respectively.

II. DESCRIPTION OF THE CIRCUIT

Circuit architecture of the proposed inverter is shown in Fig. 1, where Sak, Sbk, Sck (k = 1, 2, 2n 2) are the switching devices that serially and parallelly switch the capacitors Ck (k = 1, 2, 2n 1). The inverter bridge has the switches S1–S4. An external voltage source VIN is used as the input voltage. An inductor (L) and a capacitor (C) form the basis of a low pass filter.

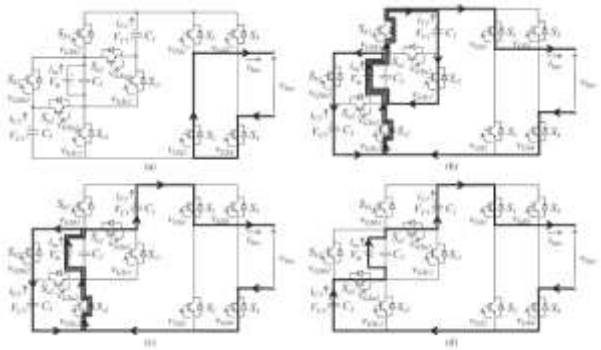

Fig. 2. Current flow of the proposed inverter (n = 2) on each state, (a) the current ibus does not flow in the capacitors Ck, (b) all capacitors are connected in parallel, (c) the capacitor C1 is connected in series and the capacitor C3 is connected in parallel, and (d) all capacitors are connected in series.

Space vector modulation [3, 12–14], multicarrier pulse width modulation (PWM) [3, 15–16], hybrid modulation [1, 3, 4, 17], selective harmonic elimination [3, 18–19], and nearest level control [3]

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are just some of the many modulation techniques that can be used to drive a multilevel inverter.

In this article, the suggested inverter is implemented using the multicarrier PWM technique.

Two examples of the suggested inverter's modulation approach are shown in Figure 3 and the current flow in Figure 2.In Fig. 3, the gate-source voltages vGS1 and vGS2 power the switches S1 and S2 when t is in the range 0 to t1. As illustrated in Fig. 3, when switches S1 and S2 are toggled back and forth, the other switches are either ON or OFF. Thus, the bus voltage vbus alternates between 0 and Vin, and the states shown in Fig. 2(a) and (b) are toggled.

In Fig. 3, the gate-source voltages vGSa1, vGSb1, and vGSc1 power the switches Sa1, Sb1, and Sc1 when t fulfills t1 t t2. As can be seen in Fig. 3, only the switches labeled Sa1, Sb1, and Sc1 are toggled between their ON and OFF positions. This results in a periodic reversal between the states shown in Fig. 2(b) and (c). In the configuration of Figure 2(b), the current iC1 charges the capacitor C1. As a result, the suggested inverter may discharge the capacitor C1 at the bus voltage vbus. In the configuration shown in Fig. 2(c), the bus voltage vbus is

$$v_{bus} = V_{in} + V_{C1}$$

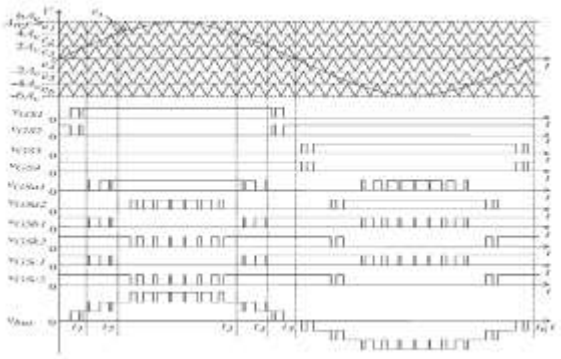

Fig. 3. Modulation method of the proposed inverter (n = 2).

where VC1 is the capacitor C1's voltage. Therefore, in this context, the suggested inverter alternates between producing Vin and producing Vin + VC1.
In Fig. 3, the gate-source voltage vGSa2 drives the switches Sa2, Sb2, and Sc2 when time t equals t2 > t > t3.

TABLE I
LIST OF THE ON-STATE SWITCHES ON EACH STATE

Relationship between e_s and e_k	On-state switches	Ideal bus voltage v_{bus}
$e_s > e_1$	S_1, S_4, S_{a1}, S_{a2}	$3V_{in}$
$e_1 \geq e_s > e_2$	$S_1, S_4, S_{a1}, S_{b2}, S_{c2}$	$2V_{in}$
$e_2 \geq e_s > e_3$	$S_1, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	V_{in}
$e_3 \geq e_s > e_4$	$S_2, S_4, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	0
$e_4 \geq e_s > e_5$	$S_2, S_3, S_{b1}, S_{c1}, S_{b2}, S_{c2}$	$-V_{in}$
$e_5 \geq e_s > e_6$	$S_2, S_3, S_{b1}, S_{c1}, S_{a2}$	$-2V_{in}$
$e_6 \geq e_s$	S_2, S_3, S_{a1}, S_{a2}	$-3V_{in}$

The vGSb2 and vGSc2 variants. As can be seen in Fig. 3, only the switches labeled Sa2, Sb2, and Sc2 are toggled between their ON and OFF positions. So, states (c) and (d) in Fig. 2 are alternated between.

During the condition shown in Fig. 2(c), the capacitor C3 is charged by the current iC3. Figure 2(d) shows the condition in which the bus voltage vbus is

$$v_{bus} = V_{in} + V_{C1} + V_{C3} \quad (2)$$

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where C3's voltage is denoted by VC3. Therefore, the suggested inverter alternates between outputting Vin + VC1 and outputting Vin + VC1 + VC3. The four states shown in Fig. 2 are cycled through indefinitely after t = t3.

When the suggested inverter (n = 2) is powered by the modulation mechanism shown in Fig. 3, the on-state switches are listed in Table I. When assuming VC1 = VC3 = Vin, the bus voltage vbus in Table I refers to the voltage at each state.

The suggested inverter uses a complete bridge linked to the high voltage, much like a standard SC inverter. As a result, the standard SC inverter stresses the other switches in the complete bridge more than the switches in the whole bridge.

The suggested inverter (n = 2) generates 7 voltage levels by cycling through the same 4 states. Capacitors C1 and C3 are discharged in equal amounts due to the alternating nature of the driving waveform seen in Fig. 3. The suggested inverter may produce a voltage waveform with 4n1 levels if the number of capacitors is n2.

Because the output voltage waveform's amplitude is inversely proportional to the double amplitude of the carrier waveform, we may define the modulation index M as follows:

$$M = A_{ref}/2A_c. \quad (3)$$

The amplitudes of the reference and carrier waves are denoted by Aref and Ac, respectively, in (3).

The suggested inverter necessitates ten switching devices for a seven-level configuration and sixteen for an eleven-level configuration. Conversely, a standard SC inverter needs 20 switching devices for a 7-level configuration and 28 for an 11-level configuration [9]. When all the dc voltage sources use the same voltage, a standard cascaded H-bridge (CHB) inverter needs 12 switching devices for the 7-level and 20 switching devices for the 11-level [17]. This means that compared to standard multilevel inverters, the proposed inverter requires fewer switching components.

III. CAPABILITY ESTIMATION

Capacitance Ck may be accurately calculated by factoring in the capacitors' voltage ripple. These capacitors are more efficient since their voltage ripple is less.

When the ripple voltage is limited to 10% of the capacitors' full voltages, the capacitance Ck is determined below.

When capacitors Ck are linked in parallel, they store energy, whereas when they are connected in series, the energy is released. As can be seen in Fig. 3, the suggested inverter (n = 2) drives its two switches, Sa1 and Sa2, symmetrically during the half cycle of the reference waveform. As a result, C1's voltage ripple is concentrated.

The suggested inverter (n = 2) has a capacitor C1 that discharges for the longest duration between times t2 and t3 in Fig. 3, assuming the output load has a power factor of cos = 1. The times t1, t2, and t3 are determined by the modulation index M, which is assumed to be 3.

$$t_1 = \frac{\sin^{-1}(1/3)}{2\pi f_{ref}} \quad (4)$$

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$$t_2 = \frac{\sin^{-1}(2/3)}{2\pi f_{ref}} \quad (5)$$

$$t_3 = \frac{\pi - \sin^{-1}(2/3)}{2\pi f_{ref}} \quad (6)$$

where fref is the reference wave's frequency.

As a result, the greatest amount of charge that may be removed from capacitor C1 is

$$Q_1 = \int_{t_2}^{t_3} I_{bus} \sin(2\pi f_{ref} t - \phi)\, dt \quad (7)$$

where Ibus is the magnitude of the bus current waveform and is the phase difference between the bus voltage and current waveforms. C1's maximum charge is assumed to be smaller than Q1. So, C1 capacitance has to meet

$$C_1 > \frac{Q_1}{0.1 V_{in}}. \quad (8)$$

Other voltage ripple induced by PWM is less than 10% when capacitors Ck fulfill (8).

It is possible to determine the capacitor IC1's peak current using

$$I_{C1} = \frac{V_{in} - V_{C1}}{r_{c1} + 2r_{on}} \quad (9)$$

where ron is the internal resistance of the switching devices and rc1 is the equivalent series resistance (ESR) of capacitor C1. Based on equation (9), the capacitor C1's peak current is equal to the input voltage Vin minus the capacitor VC1 voltage plus the switching devices' internal resistance. When C1 is big, Vin VC1 is not much of a difference in voltage. In light of this, switches with low internal resistance should be utilized.

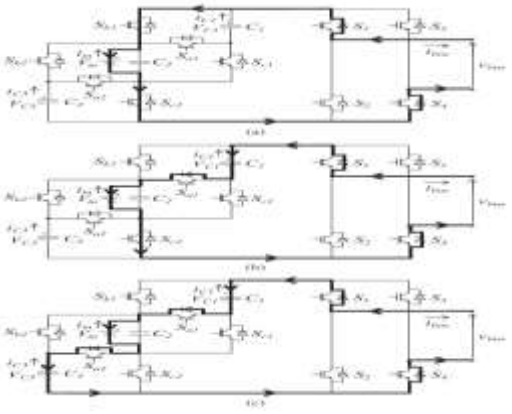

Fig. 4. Current flow of the proposed inverter (n = 2) with an inductive load,
(a) all capacitors are connected in parallel, (b) the capacitor C1 is connected in
series and the capacitor C3 is connected in parallel, and (c) all capacitors are
connected in series.

A bigger value for C1 is required to suppress the excessive peak current.

Current flows as illustrated in Fig. 4(a) and (b) before t = /2fref when the phase difference fulfills 0 sin1(2/3), or 0.745 cos 1. As illustrated in Fig. 4(b), when C1 is connected in series, the capacitor is charged by the reverse current, resulting in a higher capacitor voltage. Capacitor C1's current charge, Q_ 1, is determined by

$$Q_1' = -\int_{t_1}^{t_2} D_{Sa1}(t) I_{bus} \sin(2\pi f_{ref} t - \phi)\, dt \quad (10)$$

where Sa1's duty ratio, DSa1(t), is the variable of interest. Figure 3 shows that DSa1(t) is a sinusoid between timestamps 1 and 2. Additionally, DSa1(t1) = 0 and DSa1(t2) = 1. That's why we get DSa1(t) by

$$D_{Sa1}(t) = 3\sin(2\pi f_{ref} t) - 1. \quad (11)$$

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Based on equations (7) and (10), we may say that Q1 > Q_ 1, the charge quantity, and that Q1 > Q_ 2. Therefore, when 0.745 cos 1, Q1 controls the capacitor C1's voltage ripple.

There is a period where the current direction becomes opposite in all states of the switching devices, as seen in Fig. 4. This occurs when the power factor cos fulfills cos 0.745. Therefore, we can determine the maximum allowable discharge rate Q1 by

$$Q_1 = \int_{\frac{\phi}{2\pi f_{ref}}}^{t_0} I_{bus} \sin(2\pi f_{ref} t - \phi)\, dt. \qquad (12)$$

Reducing Q1 from its maximum discharge quantity results from Equations (7) and (12). However, with an inductive load, the input current is bigger than the reverse current, hence Q1 is more than the charge amount Q_ 1. When the power factor cos 0.745, Q1 also determines the ripple voltage across capacitor C1.

Since the peak current is proportional to the peak voltage, the maximum discharge quantity Q1 has the greatest value when cos = 1. Therefore, the suggested inverter may keep the output waveform for cos 1 when the capacitance Ck is calculated for cos = 1.

IV. LOSS ESTIMATION

The power losses of the suggested inverter (n = 2) are determined here. Losses due to switching, conduction losses of the switches, conduction loss of the output filter, and conduction losses and losses produced by the voltage ripple of the capacitors Ck are all included into the equation.

The suggested inverter has been analyzed for these losses (n = 2).

Attrition During Switching

Here, we use the charge and discharge of the parasitic capacitance to determine switching losses [20]. Based on the reference waveform es, switches S1 and S2 are turned on and off at the carrier frequency f, as shown in Fig. 3.

$$|e_s| < \frac{1}{M} A_{ref}. \qquad (13)$$

Therefore, in Fig. 3, the ON/OFF states of switches S1 and S2 occur at times t satisfying either 0 t t1 or t4 t t5.

If condition (13) is not met by the reference waveform es, switches S1 and S2 remain in their original ON or OFF states. As a result, the average number of switching transitions NS1 and NS2 in one period of reference waveform is computed as when the carrier waveforms and the reference waveform are asynchronous waveforms.

$$\overline{N_{S1}} = \overline{N_{S2}} = \frac{t_1 + (t_5 - t_4)}{t_6} \cdot \frac{2f}{f_{ref}} = \frac{2\sin^{-1}(1/M)}{2\pi} \cdot \frac{2f}{f_{ref}} \qquad (14)$$

the frequency of the switch is denoted by f. The number of switching transitions is an even number smaller than NS1 or NS1 + 4 when both the carrier and reference waveforms are synchronous waveforms. The ratio of modulated frequencies (f/fref) determines the total number of switching transitions. Therefore, separate analysis must be performed for each frequency modulation ratio when synchronous waveforms are employed in this

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modulation. Since a high switching frequency f is assumed throughout this work, the switching losses are computed using the typical number of switching transitions, denoted by the symbol NSk.

This constant reversal of meanings lasts for a whole second.

Since there are 60 seconds in a minute, NS1fref switches are flipped NS1fref times and NS2fref switches are flipped NS2fref times. The same logic applies to the S3 and S4 toggles as well. In a single switching operation, energy is lost (denoted by the symbol Eloss in the following equation) [20].

$$E_{loss} = \frac{1}{2} C_s V_{in}^2 \qquad (15)$$

where Cs is the switching devices' parasitic capacitance.

Since then, we have the following expression for the switching losses PSk (k = 1, 2, 3, 4) of these switches.

$$P_{Sk} = \frac{2\sin^{-1}(1/M)}{2\pi} \cdot C_s V_{in}^2 f. \qquad (16$$

The reference waveform alternates between cycling through the states of the switches Sak, Sbk, and Sck (k = 1, 2). The half-cycle of the reference waveform may be used to determine the switching losses of these switches. Using the same technique as in (16), we can calculate the switching losses of the switches Sak, Sbk, and Sck (k = 1, 2) as follows: (Ignoring the voltage ripple of the capacitors Ck, i.e. assuming VCk = Vin).

$$P_{Sa1} = P_{Sb1} = P_{Sc1} = \frac{2\left\{\sin^{-1}(2/M) - \sin^{-1}(1/M)\right\}}{\pi} \cdot C_s V_{in}^2 f \qquad (17)$$

$$P_{Sa2} = P_{Sb2} = P_{Sc2} = \frac{\pi - 2\sin^{-1}(2/M)}{\pi} \cdot C_s V_{in}^2 f. \quad (18)$$

When each device's voltage reaches Vin, all switches are flipped. As a result, the suggested inverter has lower switching losses than a typical full bridge inverter fed by a single voltage source.

Switches' Conduction Losses

As can be seen in Fig. 2, the proposed inverter (n = 2) may operate in one of three different configurations, or "states:" with all capacitors linked in parallel, with only one capacitor connected in series, or with all capacitors connected in series. Nonetheless, it can be shown in Fig. 2 that the bus current ibus passes via 4 switches for each condition. Thus, the overall switch conduction loss Psr may be determined by

$$P_{sr} = 4 \cdot \frac{2\pi f_{ref}}{\pi} \int_0^{\frac{\pi}{2\pi f_{ref}}} r_{on} i_{bus}^2 \, dt \qquad (19)$$

where ron represents the on-board resistance of the switch.

However, in the standard 7-level CHB inverter, current travels via 6 switches since there are 2 H-bridges. Therefore, the overall switch conduction loss of a standard 7-level CHB inverter PCHB is determined by the formula:

$$P_{CHB} = 6 \cdot \frac{2\pi f_{ref}}{\pi} \int_0^{\frac{\pi}{2\pi f_{ref}}} r_{on} i_{bus}^2 \, dt. \qquad (20)$$

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Conduction losses of the proposed inverter are lower than those of the standard 7-level CHB inverter when the identical switching devices are used, as shown by equations (19) and (20).

Output Filter Conductive Loss, Type C

Filter inductance Pl and capacitance Pc conduction losses are found using the following equations:

$$P_l = r_l i_{bus}^2 \qquad (21)$$

$$P_c = r_c i_c^2. \qquad (22)$$

The equivalent series resistance (ESR) of the filter inductance L is denoted by rl in (21). In (22), rc and ic represent the equivalent series resistance and current of the C. D. filter, respectively. Capacitor Ck Losses

Losses arise due to the discrepancy between the input voltage Vin and the capacitor voltages VCk when capacitors Ck(k _= 2) are connected in parallel. The capacitors' voltage ripple, denoted by, is determined by

$$\Delta V_k = \frac{1}{C_k} \int_{t_2}^{t_3} i_{Ck}\, dt \qquad (23)$$

where t2, t3 are times when capacitors Ck are linked in series as indicated in Fig. 3, and iCk represents the current through capacitor Ck. Therefore, the following equation may be used to determine the losses Prip caused by this voltage ripple:

$$P_{rip} = \sum_{k=1}^{2n-1} C_k \Delta V_k^2 f_{ref}. \qquad (24)$$

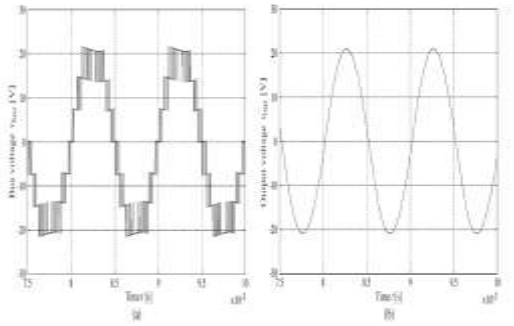

Fig. 5. Simulated voltage waveforms of the proposed inverter (n = 2) designed for low power at 5.76 [W], switching frequency f = 40 [kHz] and reference waveform frequency fref = 1 [kHz]. (a) Bus voltage waveform vbus and (b) the output voltage waveform vout.

According to the expressions (23) and (24), the efficiency increases as the capacitance grows since the loss Prip decreases.

The internal resistance rsc is responsible for the losses when many capacitors Ck are linked in series. The following equation is used to determine the Psc conduction losses of various capacitors.

$$P_{sc} = \frac{2\pi f_{ref}}{\pi} \sum_{k=1}^{2(n-1)} \int_{\frac{\sin^{-1}(2/3)}{2\pi f_{ref}}}^{\frac{\pi - \sin^{-1}(2/3)}{2\pi f_{ref}}} r_{sc} i_{Ck}^2\, dt. \qquad (25)$$

V. RESULTS OF THE SIMULATIONS

To compare the two scenarios, a simulation was run. The first scenario matched the experimental circuit conditions and concerned a low power inverter. A high-power inverter was the purpose of the other.

The low power inverter model was run in MATLAB/SIMULINK version R2009a with the following parameters.

The switching elements were models of metal-oxide semiconductor field-effect transistors (MOSFETs) with internal resistance Ron = 0.54 [] and snubber

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resistance Rs = 105 []. Filter capacitance C = 0.450 [F] and filter inductance L = 1.13 [mH]; input voltage Vin = 8.00 [V]; output resistance R = 50.0 []; modulation index M = 3.00 [kHz]; switching frequency f = 40.0 [kHz]; reference waveform frequency fref = 1.00 [kHz]. Capacitances C1 and C3 are equal to 143 [F] and 800 [m], respectively, from ESR calculations using Equation (8).

Voltage waveforms generated by the suggested inverter's (n = 2) simulation at a low power consumption of 5.76 [W] are shown in Fig. 5.

Capacitor VCk voltages are varied from 6.73 V to 7.51 V. At t = 8.11 - to 8.40 [ms] in Fig. 5(a), the voltage of the step in the bus voltage waveform falls to almost 90%. The 10% voltage loss at the Ck capacitors is to blame. The theoretical analysis confirms this. Theoretical output waveform amplitude is

$$MV_{in} = 24\ [\mathrm{V}]. \tag{26}$$

The theoretical amplitude of the output waveform is larger than the simulated amplitude, as seen in Fig. 5(b) and (26). The drop in capacitor voltage, Ck, is also a contributing factor.

The following settings were used for the high power inverter simulation. The switching devices were IGBT/Diode types with an internal resistance Ron = 65.0 [m] and a snubber resistance Rs = 105 []. Vin = 100V, R = 10R, C = 2.25CF, L = 225H, M = 3.00, f = 40.0kHz, fref = 1kHz. C1 = C3 = 712 [F] is the result of (8) for C1 and C3. Both of these capacitors, rc1 and rc3, have ESRs of 100 [m].

The simulation results for the proposed high-power inverter (n = 2) at 4.50 [kW] are shown in Fig. 6.

Capacitors VCk have their voltages adjusted between 87.0 and 97.2 volts. At t = 8.11 - to 8.40 [ms] in Fig. 6(a), the voltage of the step in the bus voltage waveform declines to nearly 90%, which is consistent with the simulation result in low power models. Theoretical output waveform amplitude is

$$MV_{in} = 300\ [\mathrm{V}]. \tag{27}$$

The theoretical amplitude of the output waveform is larger than the simulated amplitude, as seen in Fig. 6(b) and (27). The bus voltage waveform shows the reduced voltage of the capacitors Ck as the consequence of the simulation in low power models.

Current waveforms of the proposed inverter's capacitor C1 are shown in Fig. 7 through simulation. Calculating the peak current through C1 using (9) and the capacitor's voltage yields values of 0.676 [A] and 56.5 [A] for the low power and high power simulations, respectively. However, the peak currents found in the simulations had absolute values of 0.605 [A] and 52.3 [A], respectively. The nonlinear nature of the switching device models in MATLAB/SIMULINK is responsible for the discrepancies between the theoretical currents and the simulation results.

The basic component normalized simulated spectra of the bus voltage waveform are shown in Fig. 8.

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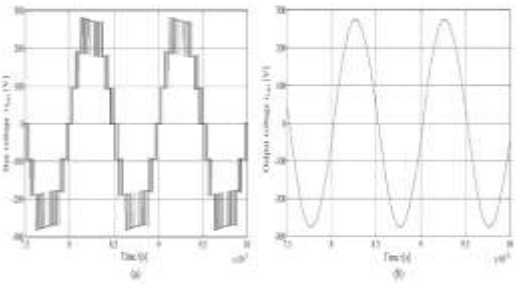

Fig. 6. Simulated voltage waveforms of the proposed inverter (n = 2) designed for high power at 4.50 [kW], switching frequency f = 40 [kHz] and reference waveform frequency fref = 1 [kHz]. (a) Bus voltage waveform vbus and (b) the output voltage waveform vout.

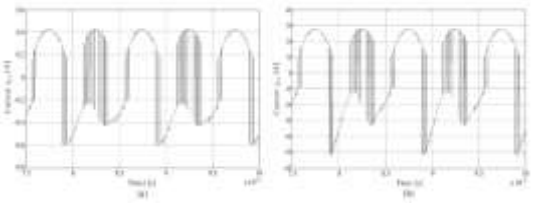

Fig. 7. Simulated current waveforms of the capacitor iC1 in the proposed inverter (n = 2).(a) Designed for low power at 5.76 [W] and (b) designed for high power at 4.50 [kW].

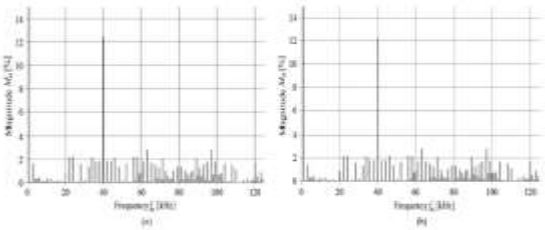

Fig. 8. Simulated spectra of the bus voltage waveform of the proposed inverters (n = 2) normalized with the fundamental component. (a) Designed for low power at 5.76 [W] and (b) designed for high power at 4.50 [kW].

The magnitude at 40 [kHz] is bigger than the other frequency components in the spectra of the bus voltage waveforms for both the low power and high power proposed inverters. The f = 40 [kHz] switching frequency is to blame for this phenomenon. The 5.76 [W] inverter and the 4.50 [kW] inverter have respective THDs of 18.9 and 18.7 percent, respectively. However, when running the same low-power simulation with a standard voltage source single-phase full-bridge inverter, its THD rises to 64.3%. Compared to a standard single-phase full-bridge inverter, the THDs of the suggested inverters are lower.

In the same conditions as the low power inverter simulation, the waveforms of the output voltage are shown in Fig. 9. As an example of an inductive load, we have a series connection between the load inductance LR = 4.89 [mH] and the load resistance R = 40.0 []. For an inductive load, the power factor is

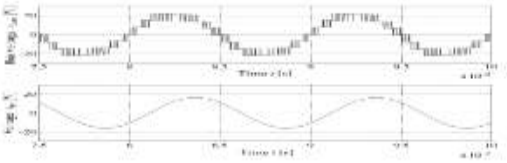

Fig. 9. Simulated bus voltage waveforms vbus and the voltage waveforms of the load resistance vR of the proposed inverter (n = 2) designed for low power at 5.76 [W] with an inductive load.

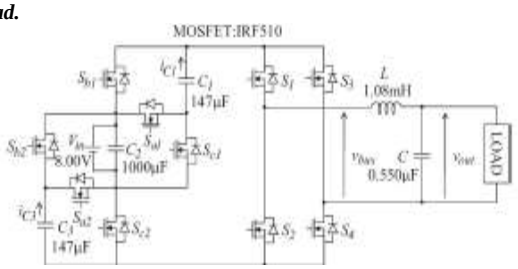

Fig. 10. Experimental circuit.

cos φ = 0.793. The inductive load may be used with the suggested inverter, as shown in Fig. 9.

VI. RESULTS OF EXPERIMENTS

An experimental setup is shown in Fig. 10. The IRF510 MOSFETs were utilized as the switch components. Both C1 and C3 were electrolytic capacitors with a 147 [F] rating and an ESR of rck = 763 [m]. To dampen the voltage source Vin's ripple current, a 1000 [F] electrolytic capacitor served as C2. Vin was drawn from a

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controlled dc power supply, namely a TP035-2D. The input voltage Vin is 8 volts, the output resistance R is 49.7 ohms, the modulation index M is 3, the switching frequency f is 40.0 kilohertz, and the reference waveform frequency fref is 1 kilohertz.

The waveform of the bus voltage, vbus, as measured in the circuit experiment is shown in Fig. 11. Figure 5(a) shows the distorted voltage waveform that results when capacitor voltages are lowered.

The measured waveform of the output voltage is shown in Figure 12.

Theoretical output waveform amplitude is

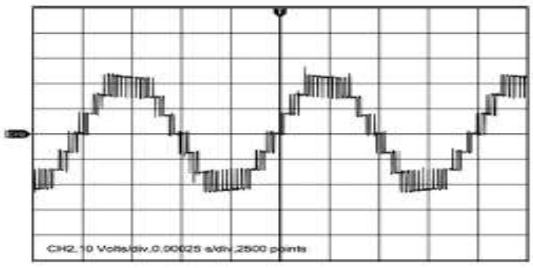

Fig. 11. Observed bus voltage waveform vbus. Vertical 10 [V/div], horizontal 250 [µs/div].

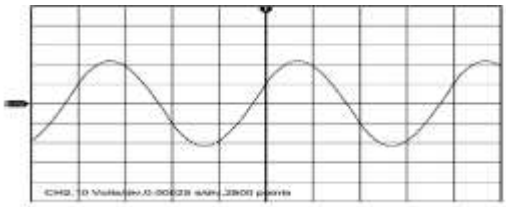

Fig. 12. Observed output voltage waveform vout. Vertical 10 [V/div], horizontal 250 [µs/div].

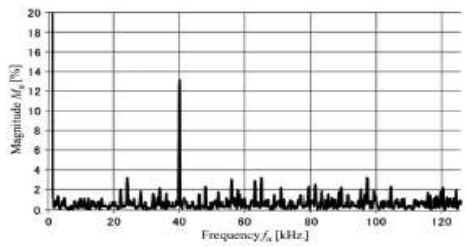

Fig. 13. Observed spectrum of the bus voltage waveform.

Under the identical conditions as the experimental circuit, the theoretical efficiency of (16)–(25) is 85.9%. It's possible that the impedance of the lines and the other resistance are to blame for the discrepancy.

The measured waveform spectrum of the bus voltage is shown in Fig. 13. The magnitudes of the lower order harmonics are tiny, as predicted by the models. The simulation findings are consistent with the THD of the bus voltage waveform being 19.5%.

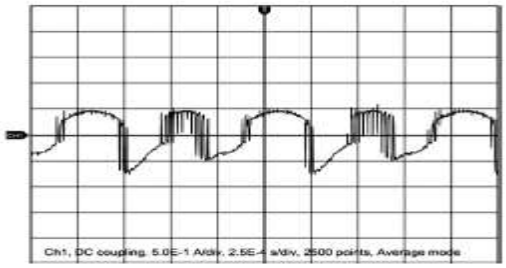

Fig. 14. Observed current waveform of the capacitor iC1. Vertical 500 [mA/div], horizontal 250 [µs/div].

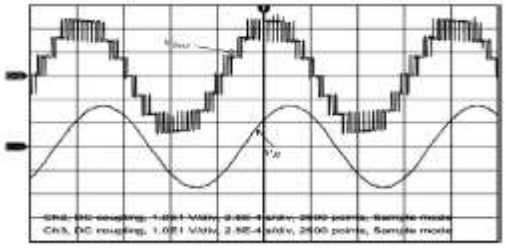

Fig. 15. Observed voltage waveforms vbus and vR with an inductive load. Vertical 10 [V/div], horizontal 250 [µs/div].

The measured current across capacitor iC1 is shown in Fig. 14. The agreement between the experimental and simulated results is shown in Figs. 7(a) and 14.

The voltage waveforms under inductive load are shown in Fig. 15. There is an inductive load consisting of a series connection between the load inductance LR = 4.89 [mH] and the load resistance R

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= 40.0 []. For an inductive load, cos = 0.793 is the power factor. As can be seen in Fig. 15, the agreement between the experimental and simulated findings was validated.

As a result, the inductive load is suitable for the suggested inverter.

VII. SUMMARY

An innovative switched-capacitor boost inverter was suggested in this study. The topology of the circuit was shown. Methods for modulation, capacitance measurement, and loss computation for the proposed inverter were shown. Results from modeling and experiments using a resistive load and an inductive load validated the inverter's circuit functioning.

By rapidly switching the capacitors between series and parallel, the proposed inverter generates an output voltage that is higher than the input voltage. An inductive load is compatible with the inverter's operation. The inverter has a more straightforward design than typical switched-capacitor inverters. The inverter's output waveform exhibits lower total harmonic distortion (THD) compared to that of a standard single-phase full-bridge inverter or a standard multilevel inverter.

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